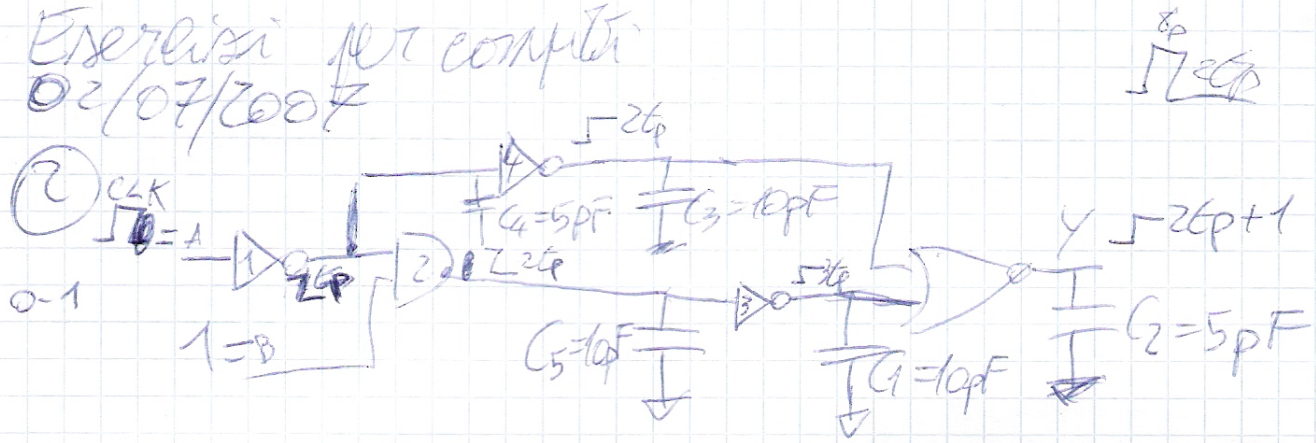
1 Aprile 2009

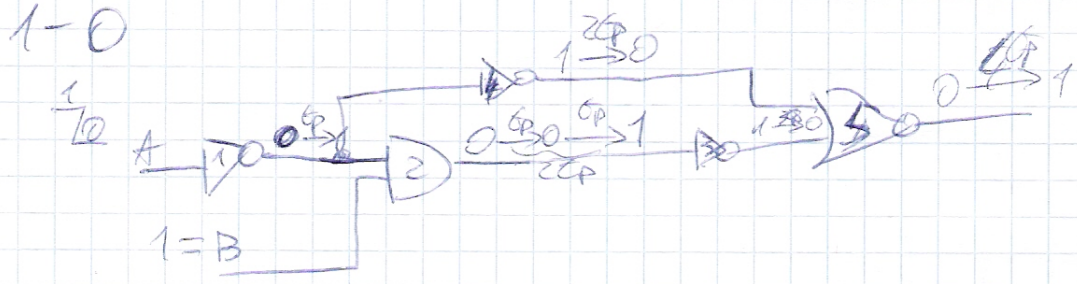
Esercizi per compiti
02/07/2007



AB	$Y = \bar{A}B + A = \bar{A}B \cdot \bar{A} = \bar{A}\bar{B} = A\bar{B}$
00	0
01	1
10	0
11	0

$\Rightarrow 3t_p = 3 \cdot 50\,ns$

AB	
00	1
01	0
10	0
11	0



$P_{D1} = 0$

$P_{D2} = f \cdot V_{DD}^2 \cdot C_L = 1 \cdot 10^6 \cdot 5V \cdot (C_5 + C_{in}) =$

$P_{D3} = f \cdot V_{DD}^2 \cdot C_L = (C_1 + C_{in}) \cdot V_{DD}^2 \cdot f$

$P_{D4} = 0$

$P_{D5} = f \cdot V_{DD}^2 \cdot (C_2)$

7/11/2008

① S_1, S_2, S_3, S_4

Y (Attivo alto)

$t = 30_5$

2 sensori attivi

E attivo alto disabilita

S_1	S_2	S_3	S_4	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

S_3S_4 \ S_1S_2	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	1	1	1	1
10	0	1	1	1

$$Y = \bar{E}S_1S_2 + \bar{E}S_3S_4 + \bar{E}S_2S_4 + \bar{E}S_1S_4 + \bar{E}S_1S_3 + \bar{E}S_2S_3$$

$$= \bar{E}\left(S_1S_2 + S_3S_4 + S_2S_4 + S_1S_4 + S_1S_3 + S_2S_3\right) =$$

$$= \bar{E}\left(S_2(S_1 + S_4) + S_3(S_1 + S_4) + \cdots\right)$$

$$+ S_1 S_4 + S_2 S_3)$$

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

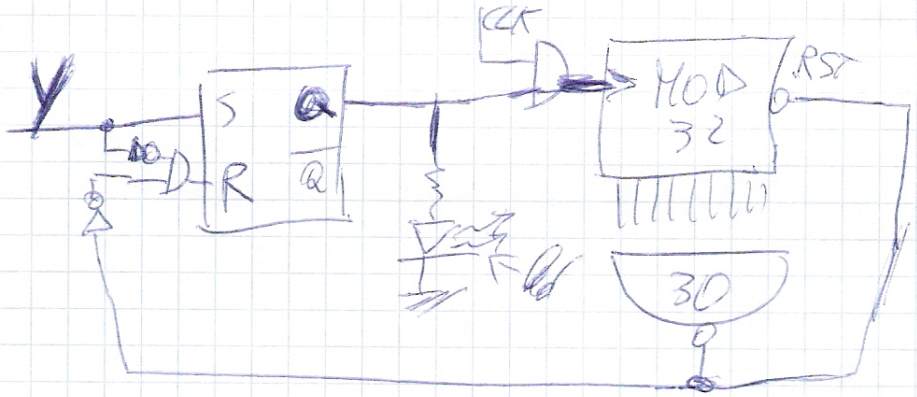
$$= \overline{E}\,(\quad)$$

$$= \overline{E} + (\quad) =$$

$$= \overline{E} + (\overline{S_1 S_2} + \overline{S_3 S_4} + \overline{S_2 S_4} + \overline{S_1 S_4} + \overline{S_1 S_3} + \overline{S_2 S_3})$$

$$= \overline{E} + [(\overline{S_1} + \overline{S_2}) + \quad)$$

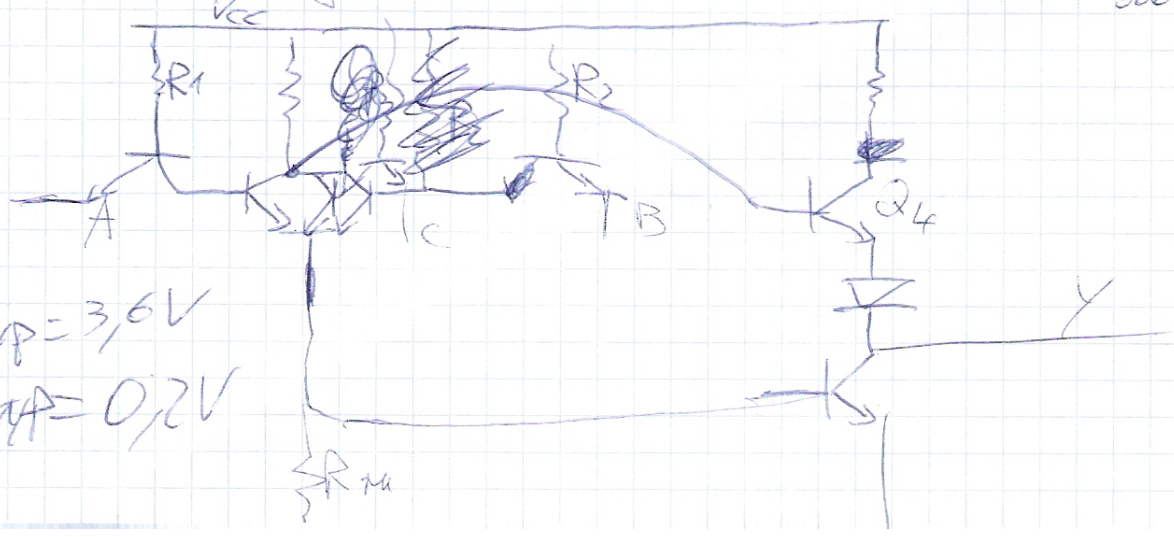
$$= E + [(\overline{S_1} + \overline{S_2}) + (\overline{S_3} + \overline{S_4}) + (\overline{S_2} + \overline{S_4}) + (\overline{S_1} + \overline{S_4})(\overline{S_1} + \overline{S_3})(\overline{S_2}$$



SIRENA

(2) NOR a 3 ingressi

TTL



$V_{OH\,typ} = 3{,}6\,V$

$V_{OL\,typ} = 0{,}2\,V$

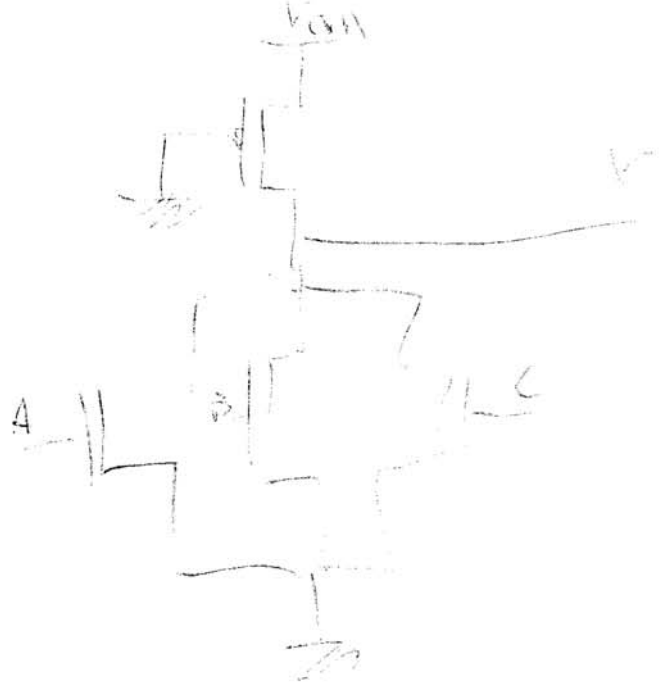
$\overline{A+B(C}$

CMOS

$V_{GS\,TP} = V_{DD}$

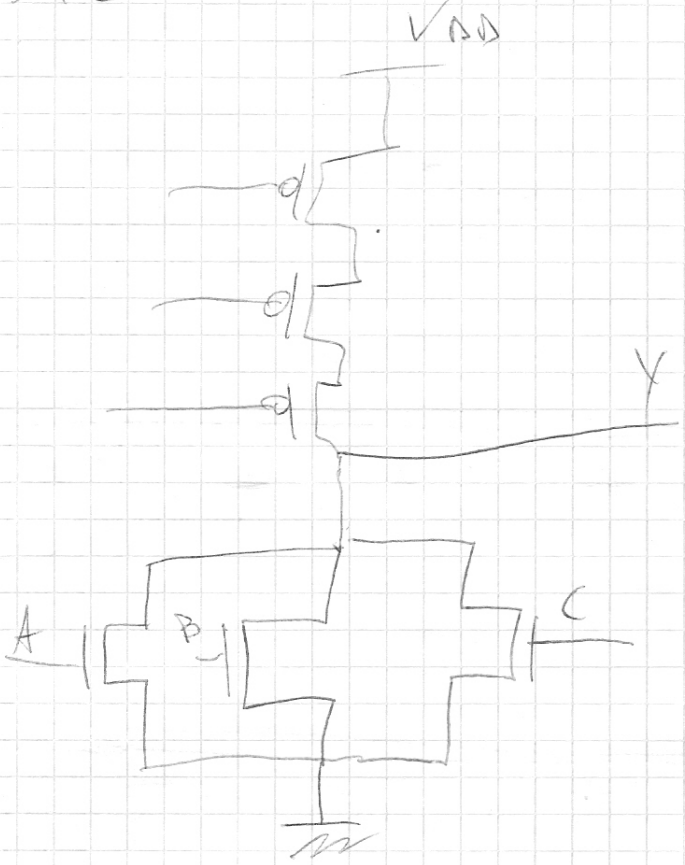
$V_{GS\,TP} = 0V$

PSEUDO NMOS



$\overline{A+B+C}$

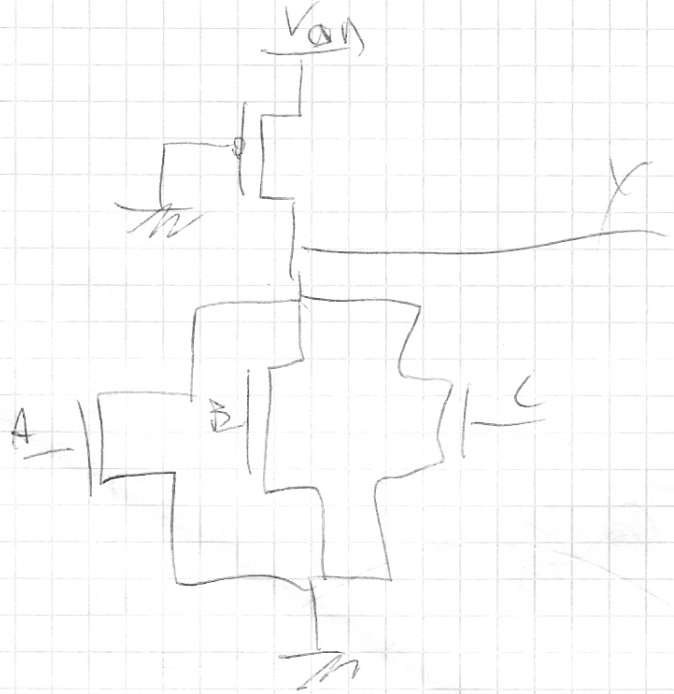
CMOS



$V_{OHTYP} = V_{DD}$

$V_{OLTYP} = 0V$

PSEUDO NMOS



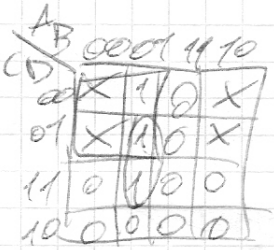
③ Flip flop D condensato con ing. asincroni

D	CLK	CLEAR	Y
0	↑	1	0
1	↑	1	1
X	X	0	0

④

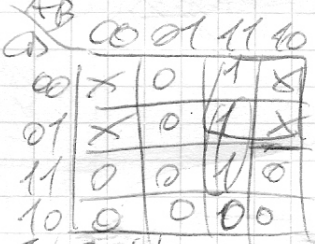
A	B	C	D	I_1	I_2	I_3	I_4
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0
1	0	0	0	X	X	X	X
1	0	0	1	X	X	X	X
1	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1
1	1	0	0	0	0	1	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	1	1
1	1	1	1	0	0	1	0

I_2:



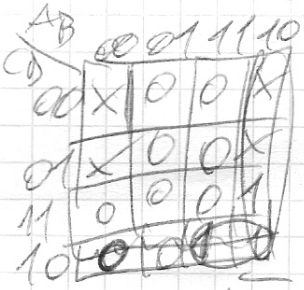
$I_2 = \bar{A}\bar{C} + A\bar{B}D$

I_3



$I_3 = A\bar{C} + \bar{A}BD$

I_4

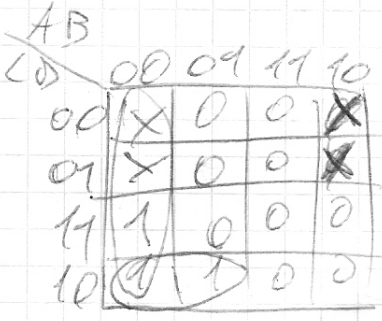


$I_4 = A\bar{B} + A\bar{C}\bar{D}$

$I_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} =$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C}\bar{D}$

I_1

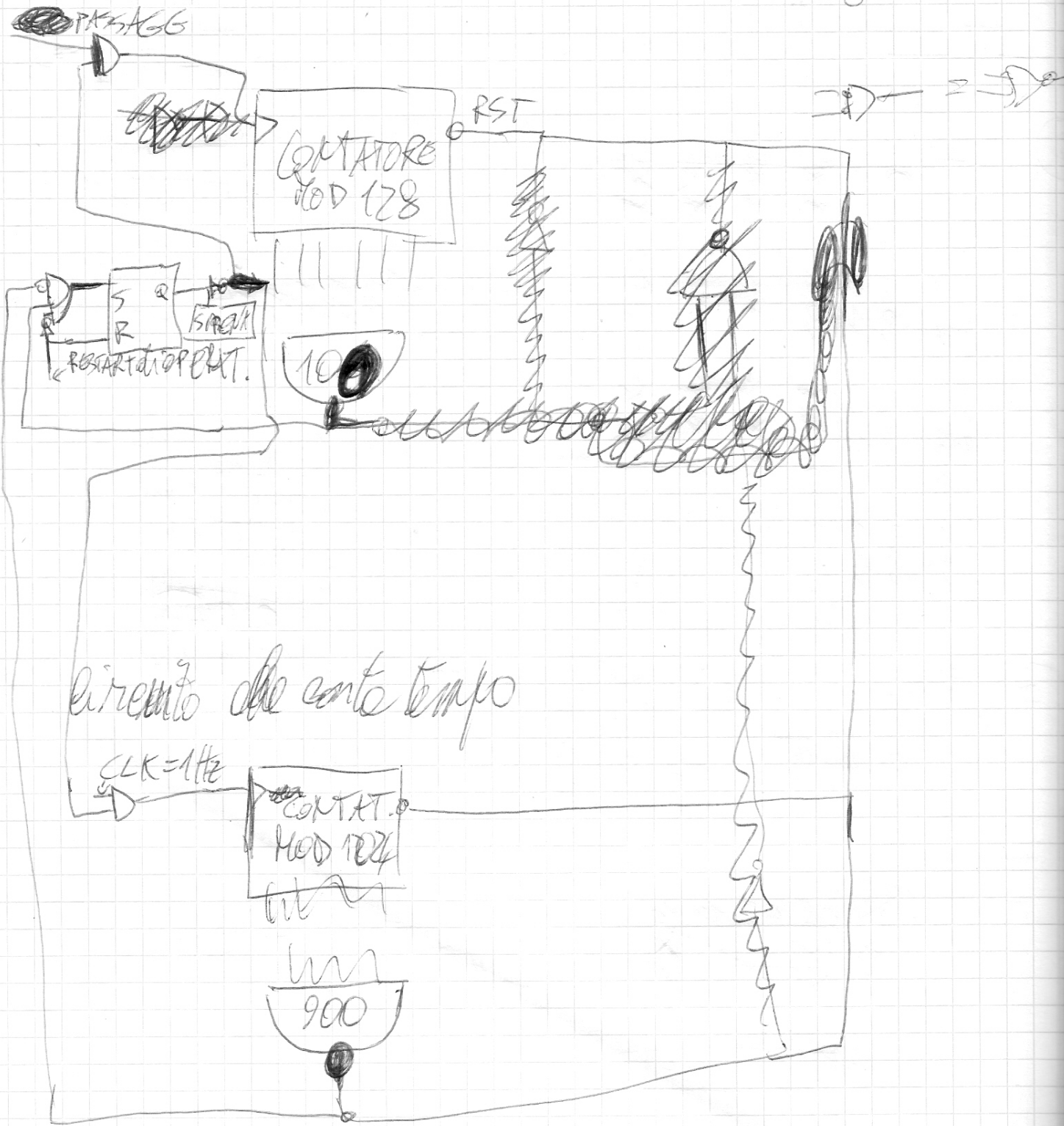


$I_1 = \bar{A}\bar{B} + \bar{A}C\bar{D}$

18/04/2008

① ogni 900 secondi

circuito che conta numero di ingressi

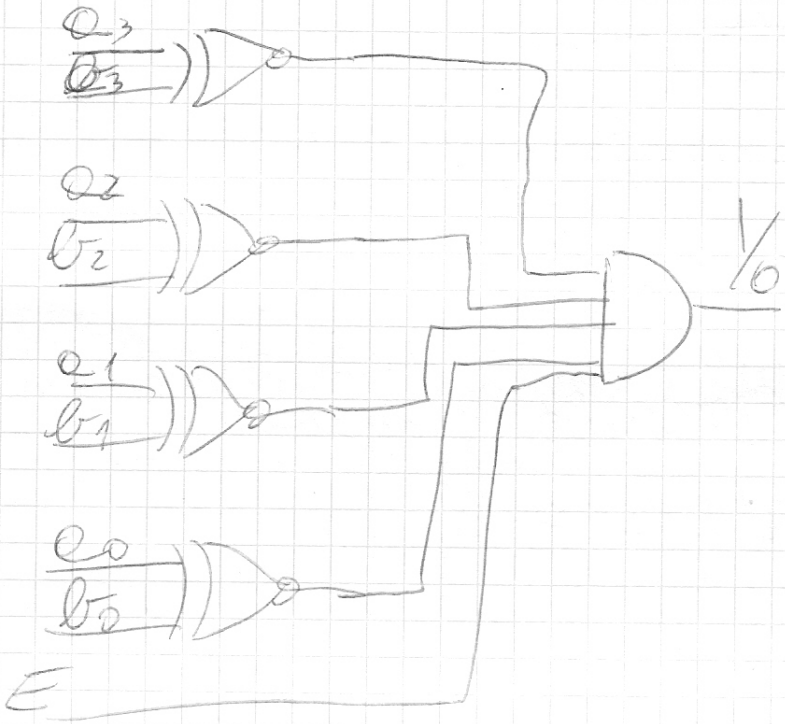


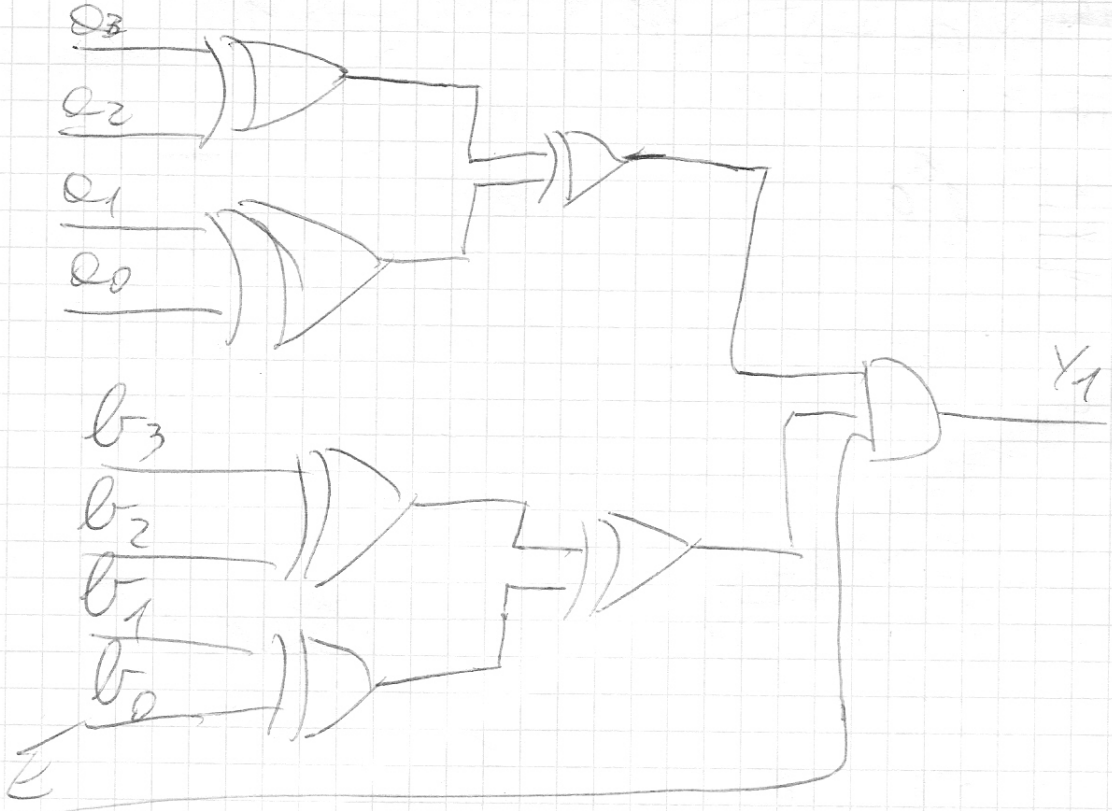
circuito che conta tempo

~~③ $Y = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B}\bar{D}$~~

④ $A = Q_3 Q_2 Q_1 Q_0$

$B = b_3 b_2 b_1 b_0$





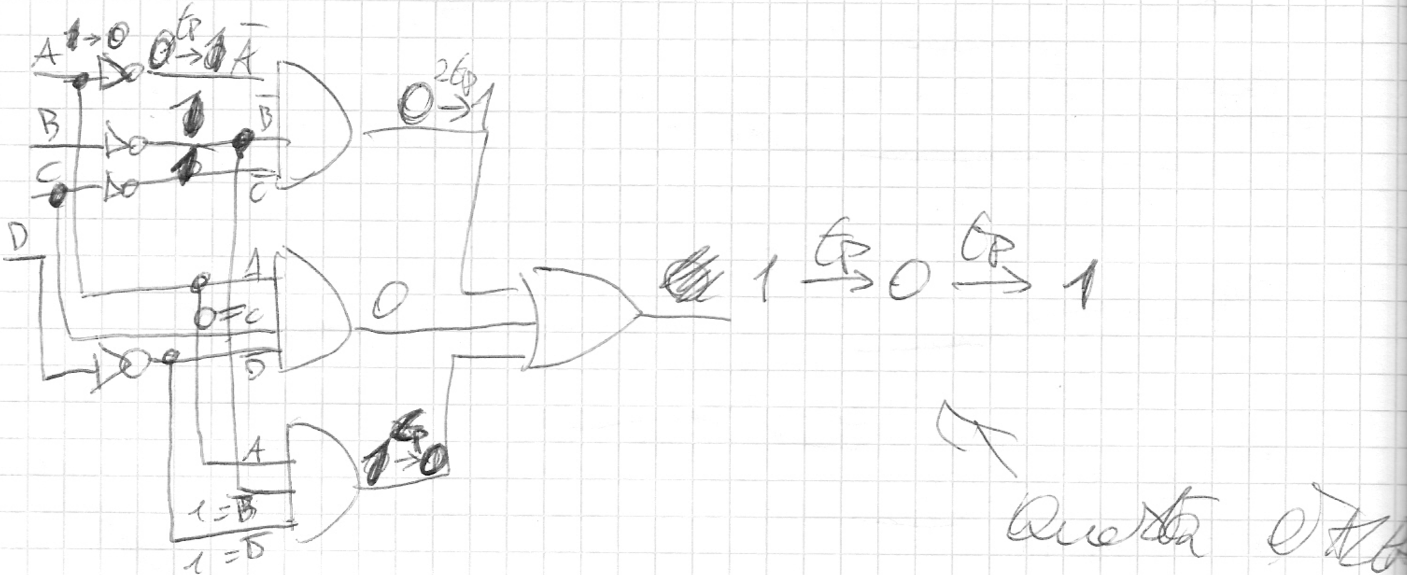
② $Y = \bar{A}\bar{B}\bar{C} + AC\bar{D} + A\bar{B}\bar{D}$

AB / CD	00	01	11	10
00	1			1
01	1			
11				
10			1	1

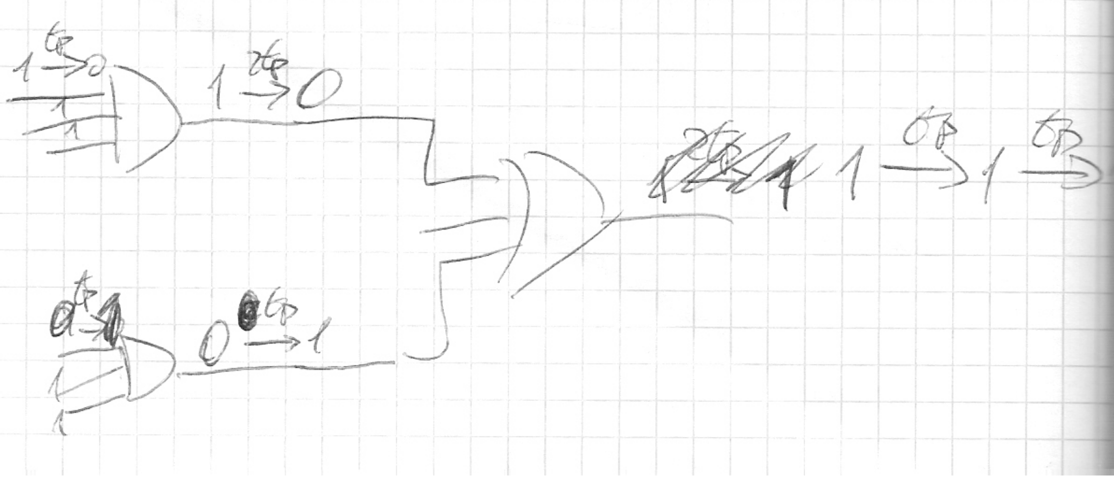
$\bar{B}\bar{C}\bar{D}$

Facciamo circuito

Tra 11→0 B=0 C=0 D=0

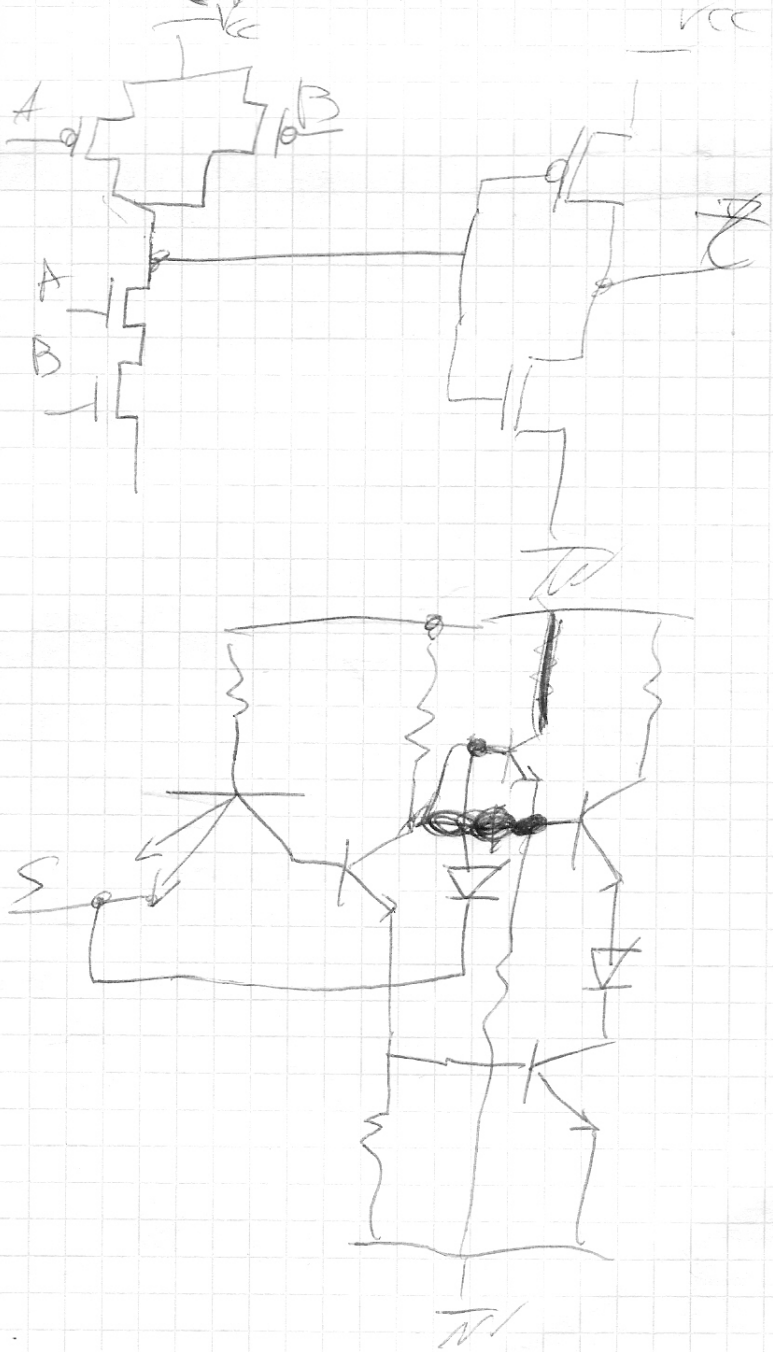


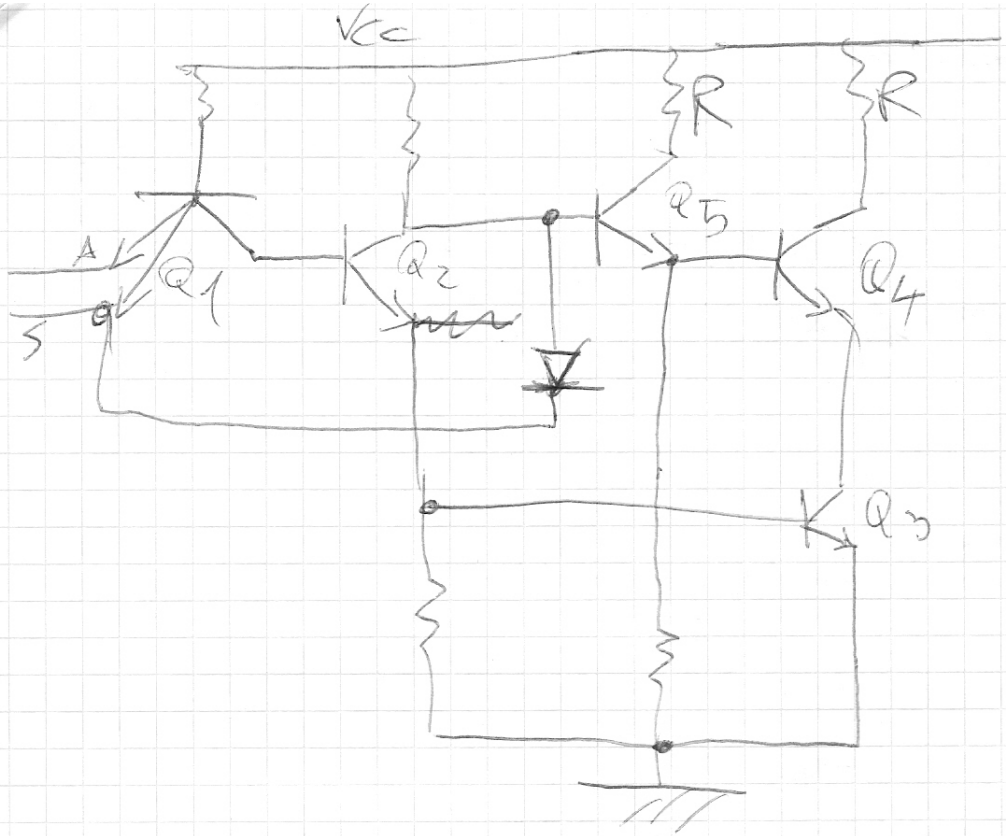
Tra 0 e 1



è stato eliminato perché attraverso ~~il~~ porte in più che sia nella transizione 0→1 che 1→0 vale sempre 1

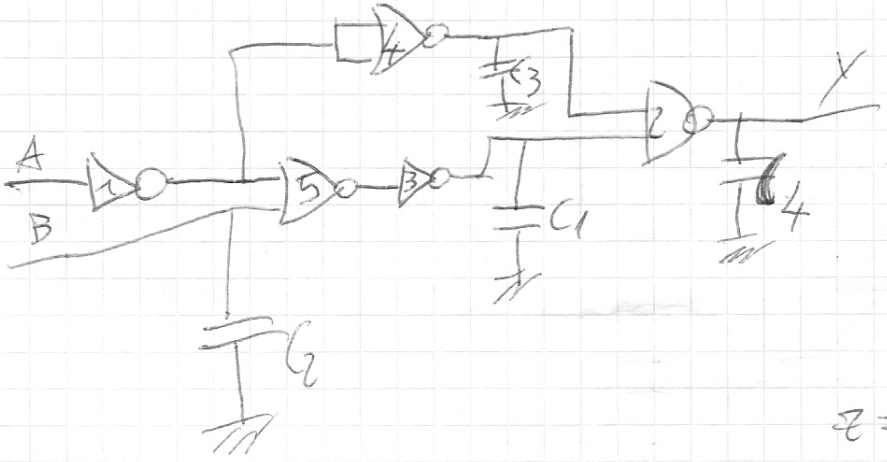
→ AB con CMOS:





16/02/2006

(3)



$\overline{Z}$

$Z = \overline{(\overline{A}+B)\cdot A} = A\overline{A} + \ldots$

$= 0 + B\overline{A}$

$= B\overline{A}$ $B=0$

A B	$Y = \overline{(\overline{A}+B)\cdot A} = \overline{(\overline{A}+B)}\cdot A = \overline{A}\cdot A + \overline{B}\cdot A = \overline{AB}$
0 0	1
0 1	1
1 0	1
1 1	0

Transizione $0 \rightarrow 1$

NOR

$A = B$

$\Rightarrow 3t_p = 150\,ns$

05/09/2005

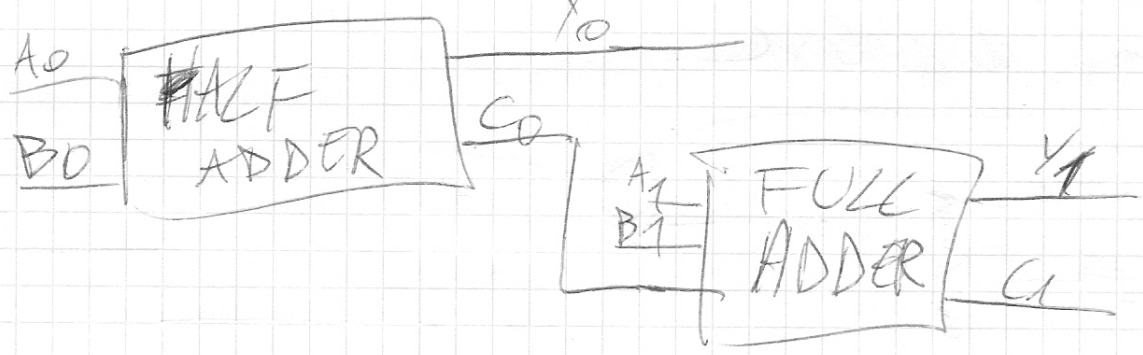
① A_1, A_0, B_1, B_0

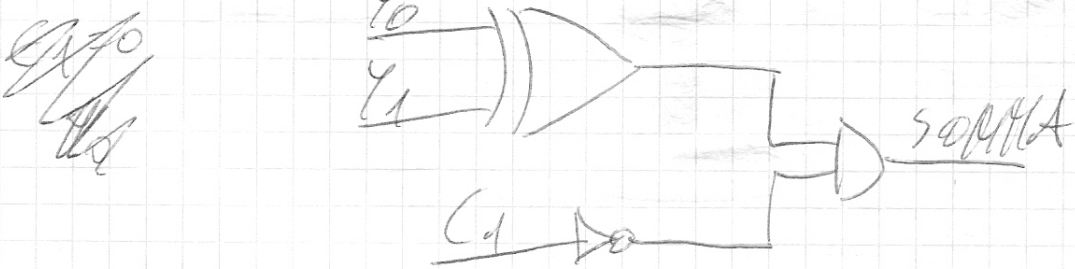
CLK e uscite U

~~A_1 A_0 B_1 B_0~~

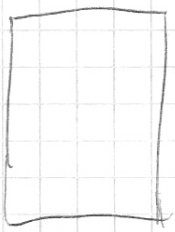
0 1
1 0

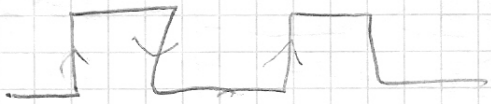
sommatore



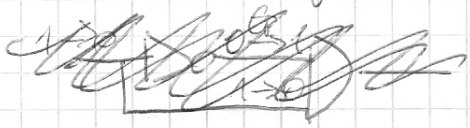


CLK con duty cycle al 50%



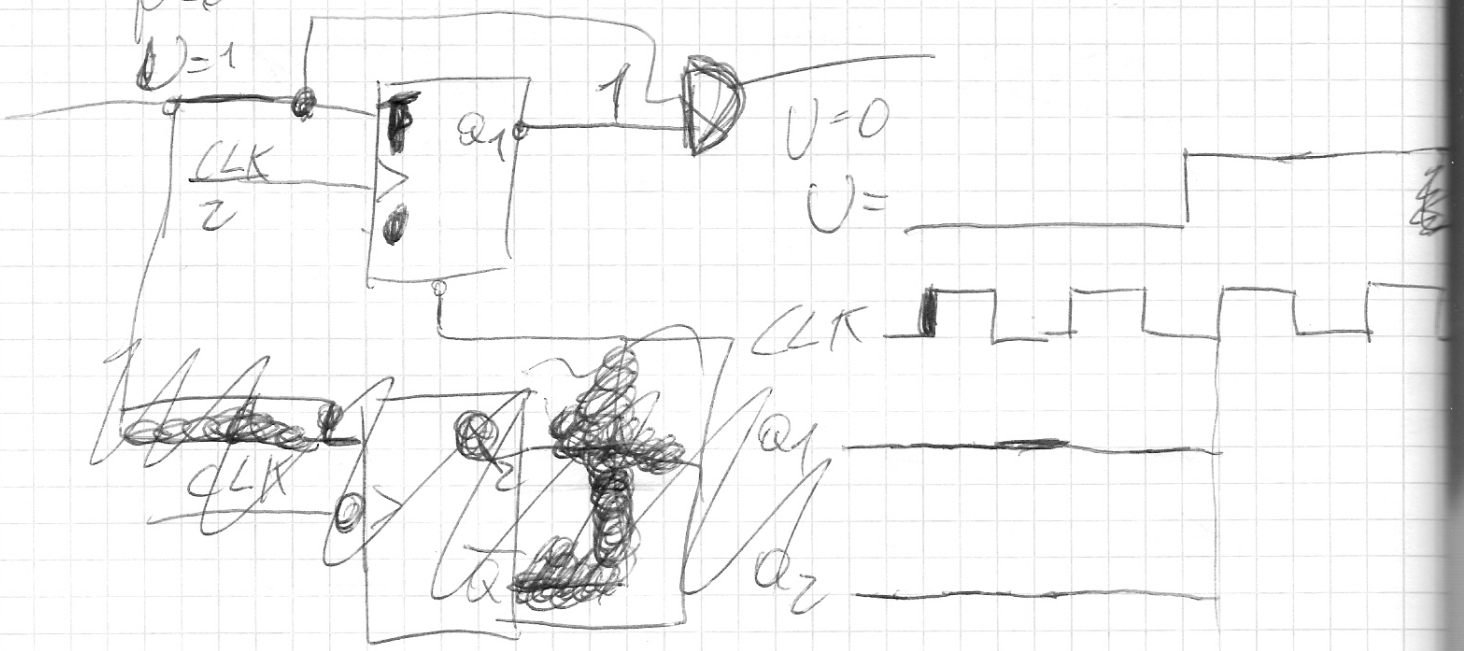


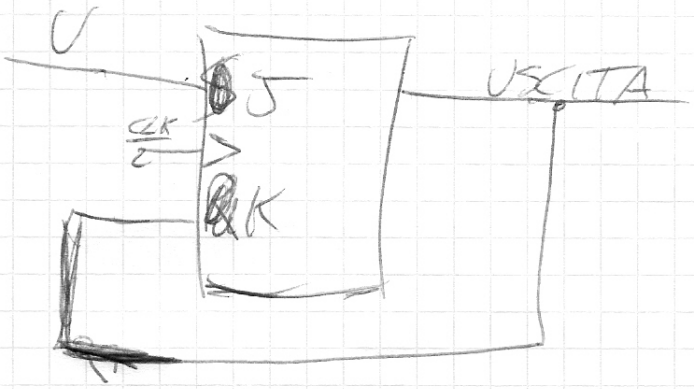
Rilevatore di fronte:



fronte di salita:

fronte di discesa




U
J
CLK
C
K
USCITA

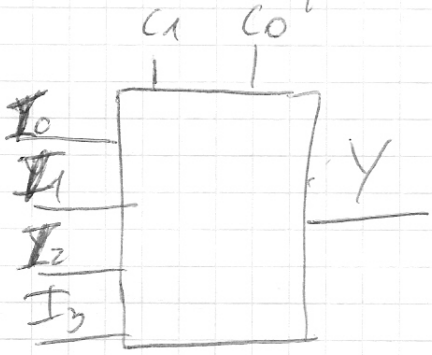
30/06/2004

② $A = a_3 a_2 a_1 a_0$

$B = b_3 b_2 b_1 b_0$

$c_1 c_0$

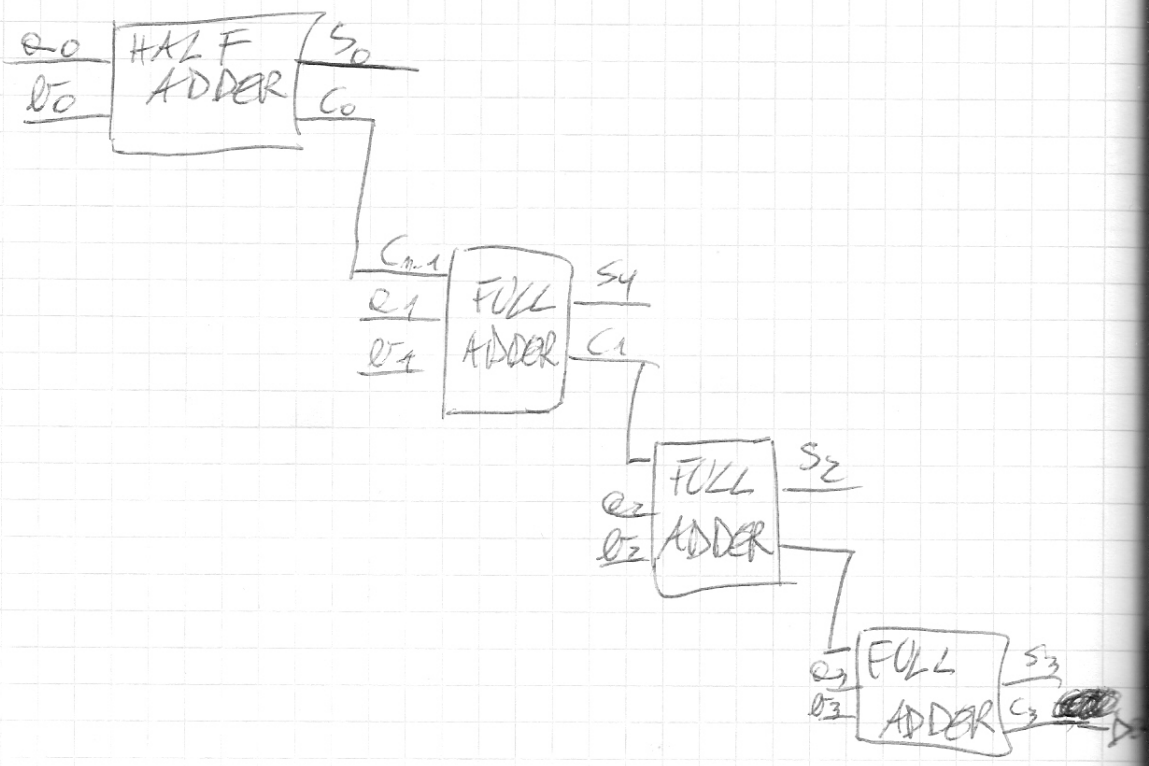
Usiamo un multiplexer



I_0 = è 1 se non c'è OVERFLOW nella somma

se c'è OVERFLOW

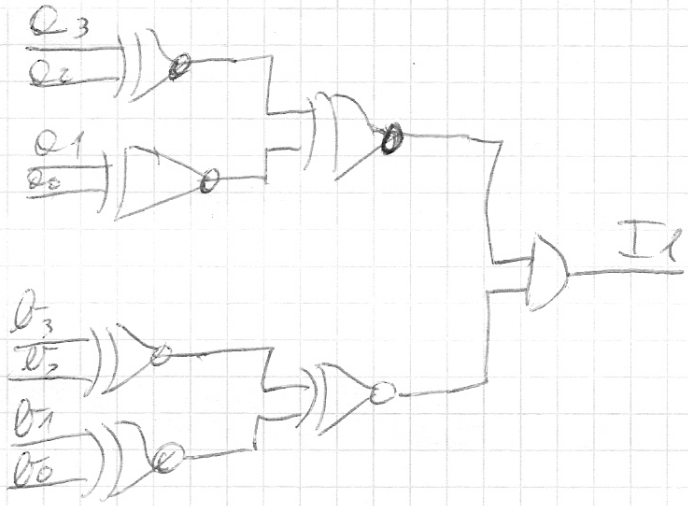
⇒ due sommatori



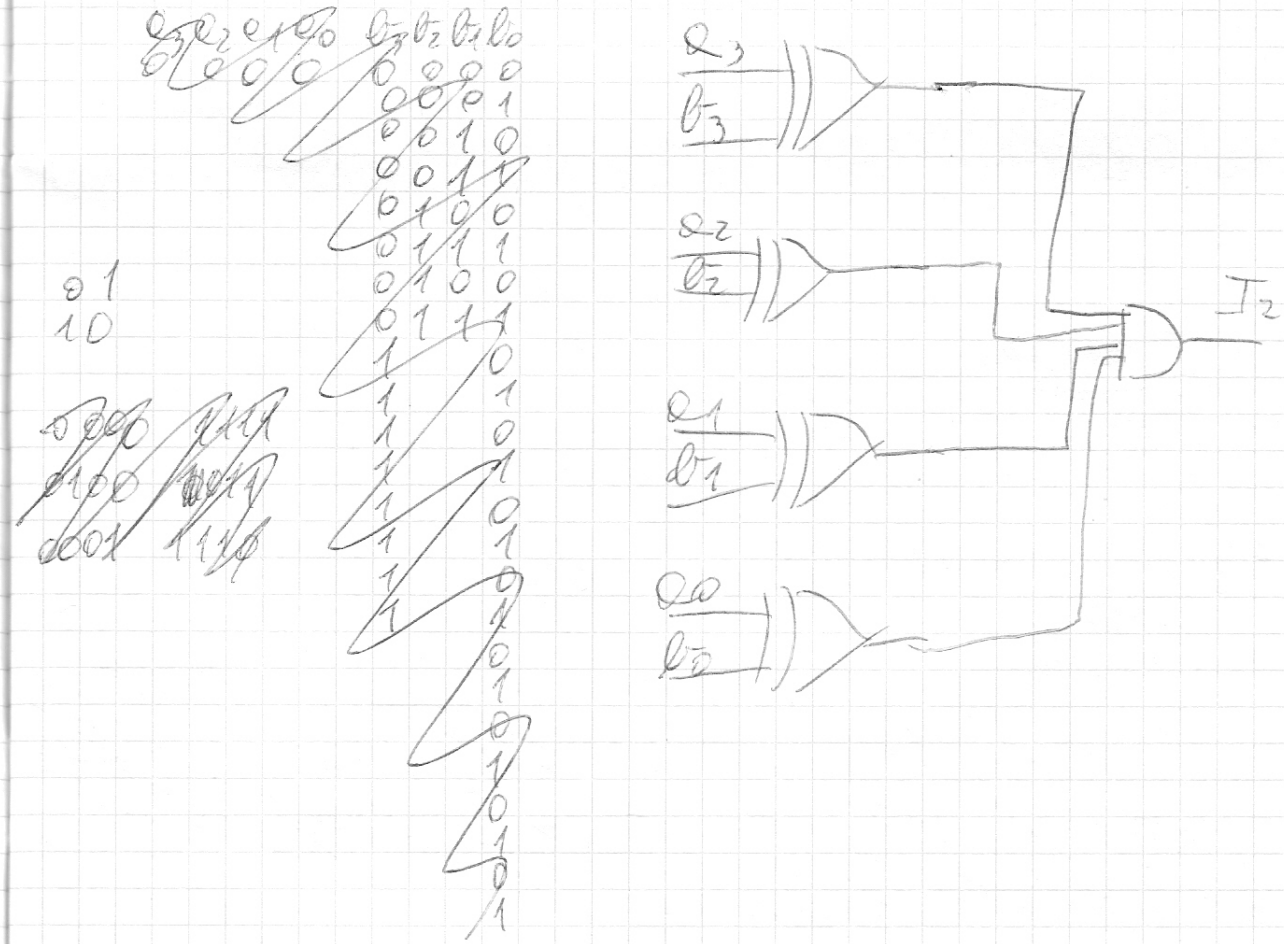
I_1 se ~~dist~~ entrambe le parole hanno numero pari di 1

Usiamo EX-OR

EX OR	EX NOR
00 0	00 1
01 1	01 0
10 1	10 0
11 0	11 1



I_2 = distanza > 3 (contiamo ~~tutte~~ tutti i bit)



I_3 =

④ • $V_{OH\,TYP}$ è la tensione ~~di uscita~~ che ~~tipicamente~~ viene riconosciuta in uscita come livello alto

CMOS $V_{OH\,TYP} = V_{DD}$

TTL $V_{OH\,TYP} = 3{,}6\,V$

• $V_{OH\,min}$

Minimo valore di tensione ~~necessario~~ che è possibile riconoscere come livello alto in uscita

CMOS: $V_{OH\,min} = V_{DD}/2$

TTL: $V_{OH\,min} = 2{,}4\,V$

• CMOS:

$NM_L = 50\% \cdot V_{DD}$

TTL

$NM_L = 0{,}4\,V$

• ~~CMOS~~ TTL

$F.O._H = \frac{400\,\mu A}{40\,\mu A} = 10$

~~TTL~~ CMOS

FO è molto elevato ma si prende 50

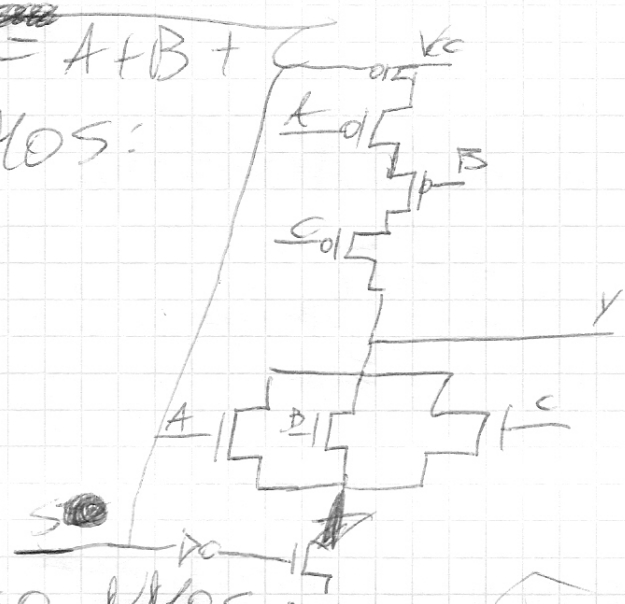
• Tempo di predisposizione: ~~tempo in cui l'ingresso deve rimanere per uno stato prima di essere realmente acquisito~~

Tempo per cui l'ingresso deve rimanere costante prima della transizione affinché non ci siano

· Numero di Mod:
numero di stati massimo esprimibile dal contatore.
Se un contatore è Mod 16 vuol dire che può contare 16 stati.

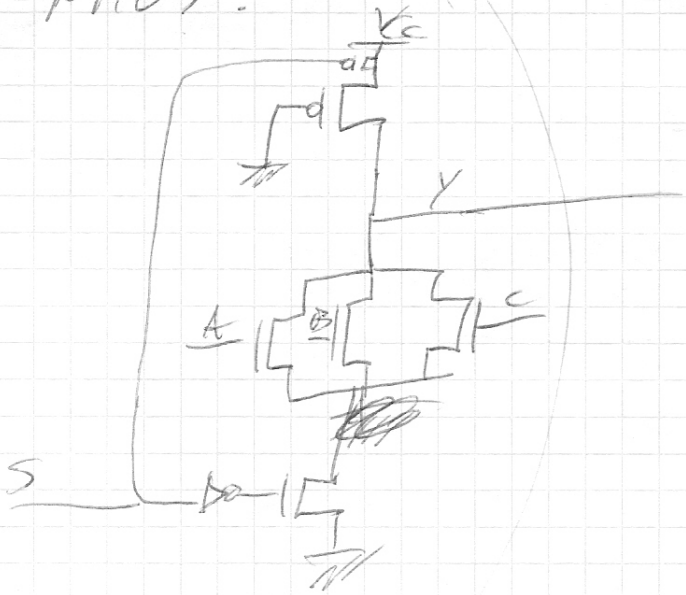
(3) $Y = A + B + C$

CMOS:



Tra questa configurazione quando tutti e 3 gli ingressi portano a livello logico basso vorrebbero attivarsi i 3 PMOS della PUN e disattivarsi gli NMOS della PDN e quindi di conseguenza all'uscita ci sarebbe VDD se invece almeno un ingresso è alto Y=0

PSEUDO-NMOS:



← Il PMOS è sempre attivo.
Se tutti gli NMOS e attivo (se almeno un ingresso è 1)
⇒ uscita vale 0

Se è un 3-stati se S vale 0 allora il circuito è in stato di alta impedenza

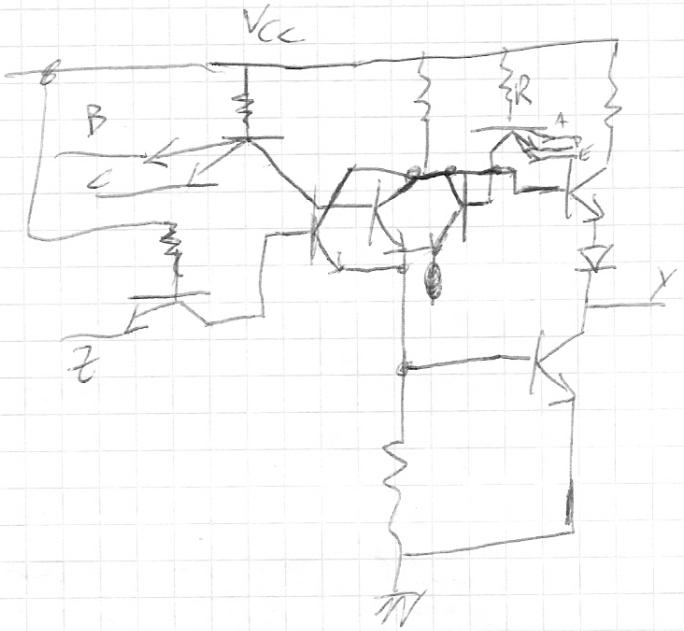
Qui c'è dissipazione di potenza statica se Y=0

TTL

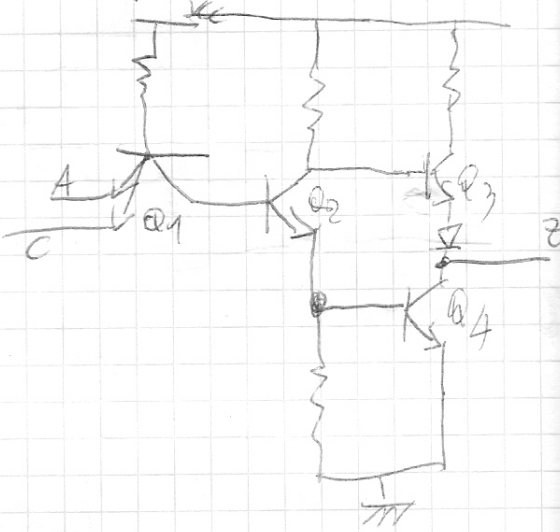
$Y = BC + A\bar{D}\bar{E} + \overline{AC}$

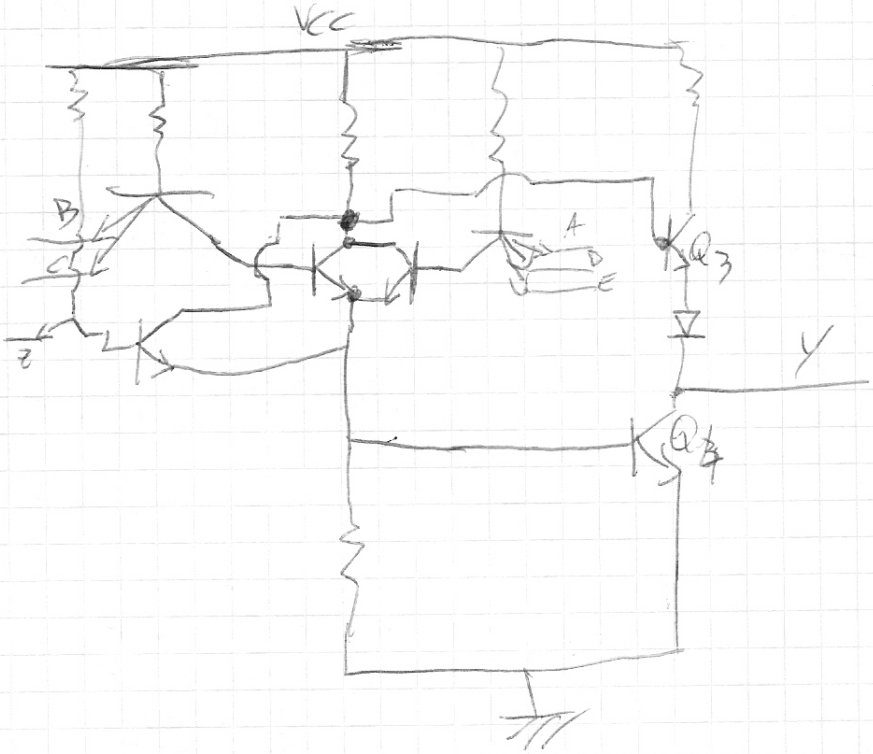
Chiamiamo $z = \overline{AC}$

$\Rightarrow$

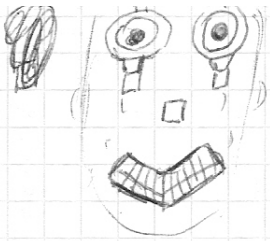


$z = \overline{AC}$

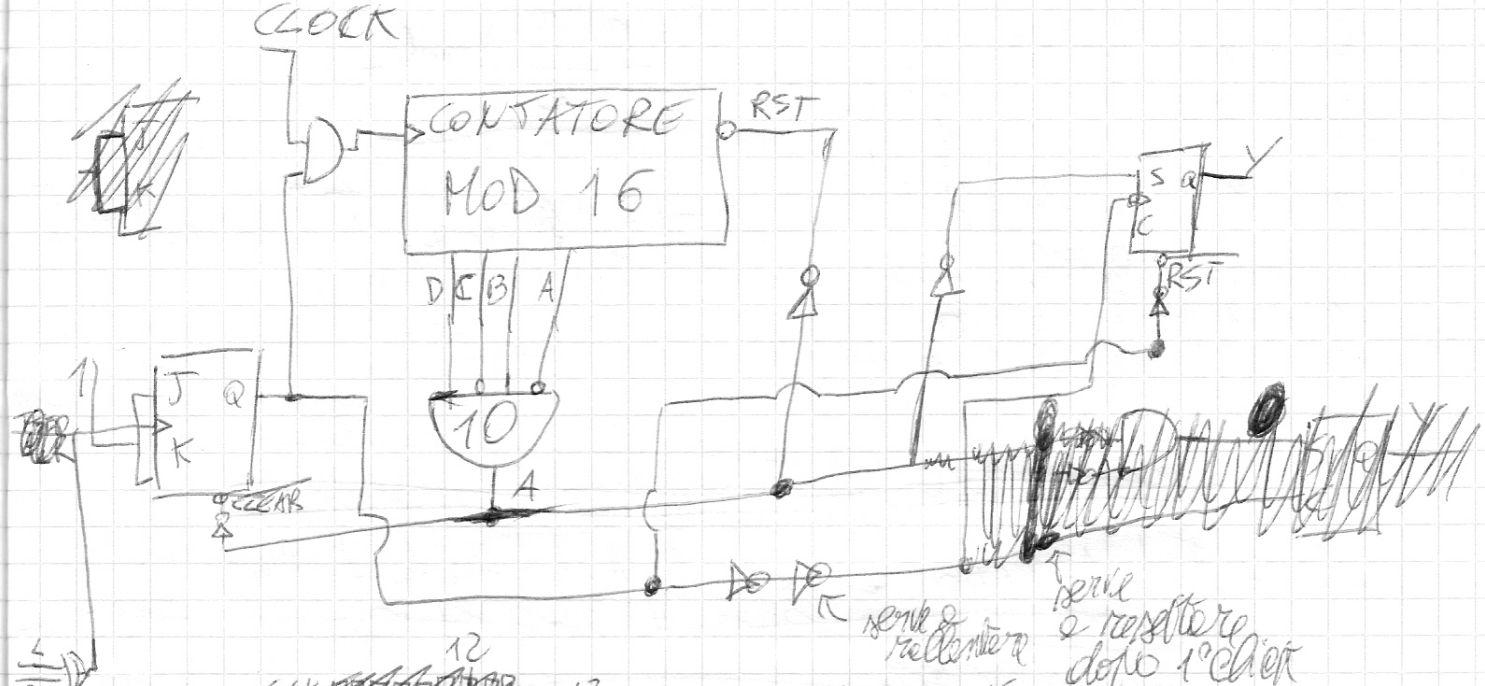


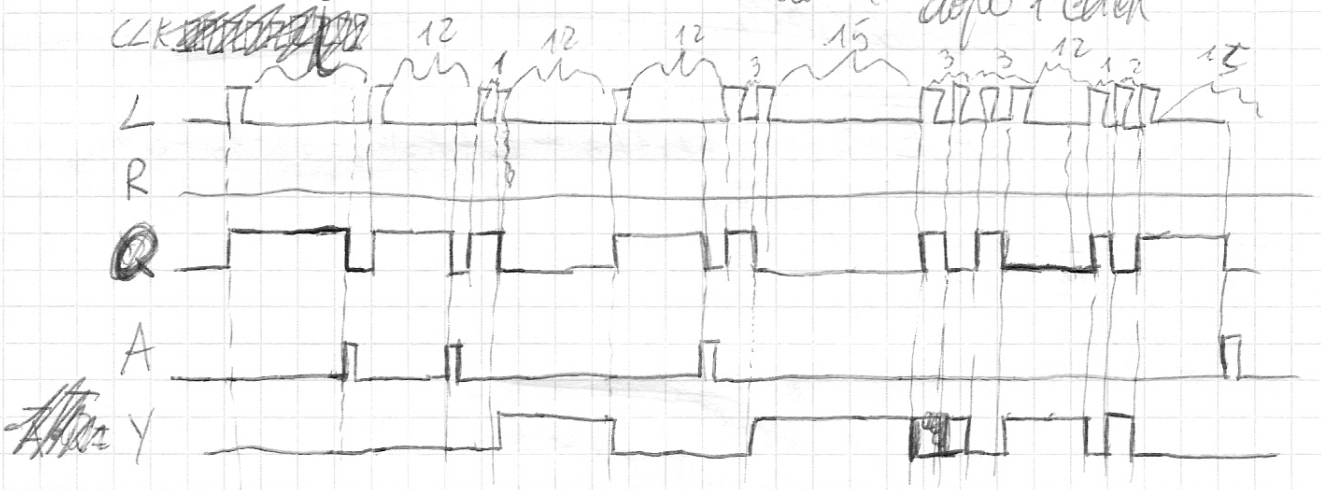


15/09/2006



① ingressi L e R uscita Y





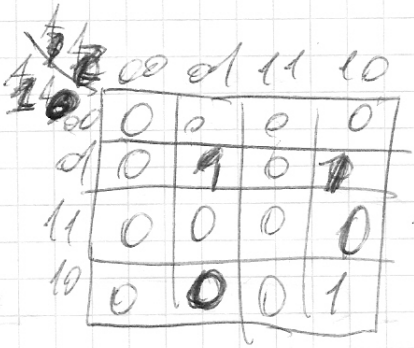
OK

② Fatto direttamente sul foglio

③

A_3	A_2	A_1	A_0	Y = 1 se almeno 2 input non adiacenti sono 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

$\bar{E}$	A_3	A_2	A_1	A_0	Y
0	×	×	×	×	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0



$Y = \bar{E}A_3A_2\bar{A}_1A_0 + \bar{E}A_3\bar{A}_2\bar{A}_1A_0 + \bar{E}A_3\bar{A}_2A_1\bar{A}_0 + \bar{E}A_3A_2A_1A_0 =$

$= \bar{E}A_3\bar{A}_0(A_2\bar{A}_1 + \bar{A}_2A_1) + \bar{E}A_3A_0(\bar{A}_2\bar{A}_1 + A_2A_1) =$

$= \bar{E}A_3\bar{A}_0(A_2 \oplus A_1) + \bar{E}A_3A_0\overline{(A_2 \oplus A_1)} =$

$= \bar{E}A_3(A_2 \oplus A_1) \cdot \overline{(A_2 \oplus A_1)} + \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)} =$

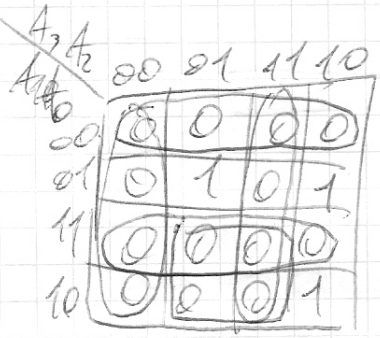
$= \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)} \cdot \overline{(A_2 \oplus A_1)} + \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)} =$

$= \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)} + \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)} =$

$= \bar{E}A_3 \cdot \overline{(A_2 \oplus A_1)}$

$\overline{A+B} = \bar{A} \cdot \bar{B}$

$\overline{A \cdot B} = \bar{A} + \bar{B}$



$Y = \bar{E}(A_3 + A_2) \cdot \bar{E}(A_1 + A_0) \cdot \bar{E}(\bar{A}_3 + \bar{A}_2) \cdot \bar{E}(\bar{A}_2 + \bar{A}_1) =$

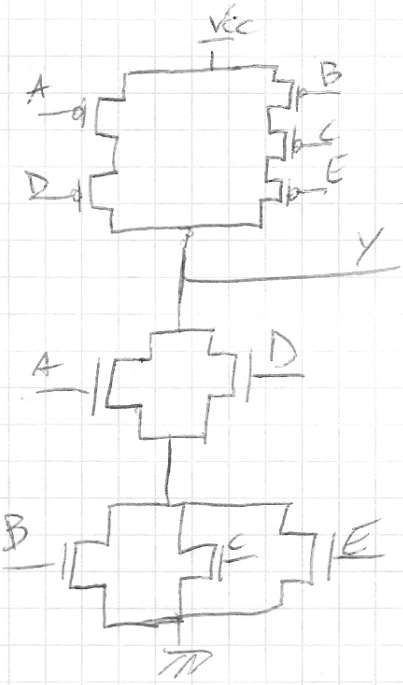
$= \overline{\bar{E}(A_3 + A_2) \cdot \bar{E}(A_1 + A_0) \cdot \bar{E}(\bar{A}_3 + \bar{A}_2) \cdot \bar{E}(\bar{A}_2 + \bar{A}_1)} =$

$= \overline{\bar{E}(A_3 + A_2)} + \overline{\bar{E}(A_1 + A_0)} + \overline{\bar{E}(\bar{A}_3 + \bar{A}_2)} + \overline{\bar{E}(\bar{A}_2 + \bar{A}_1)}$

Dobi mor

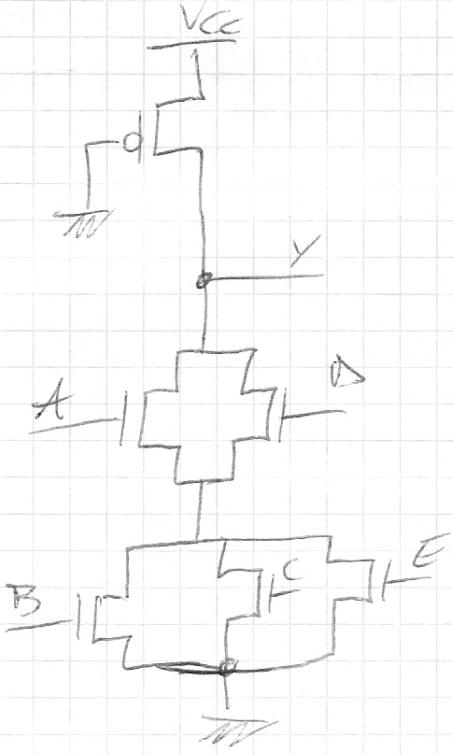
④ $Y = \overline{A}\,\overline{D} + \overline{B}\,\overline{C}\,\overline{E} = \overline{\overline{A}\,\overline{D} + \overline{B}\,\overline{C}\,\overline{E}} = \overline{\overline{A}\,\overline{D}} \cdot \overline{\overline{B}\,\overline{C}\,\overline{E}} =$

$= \overline{(A+D)\cdot(B+C+E)}$



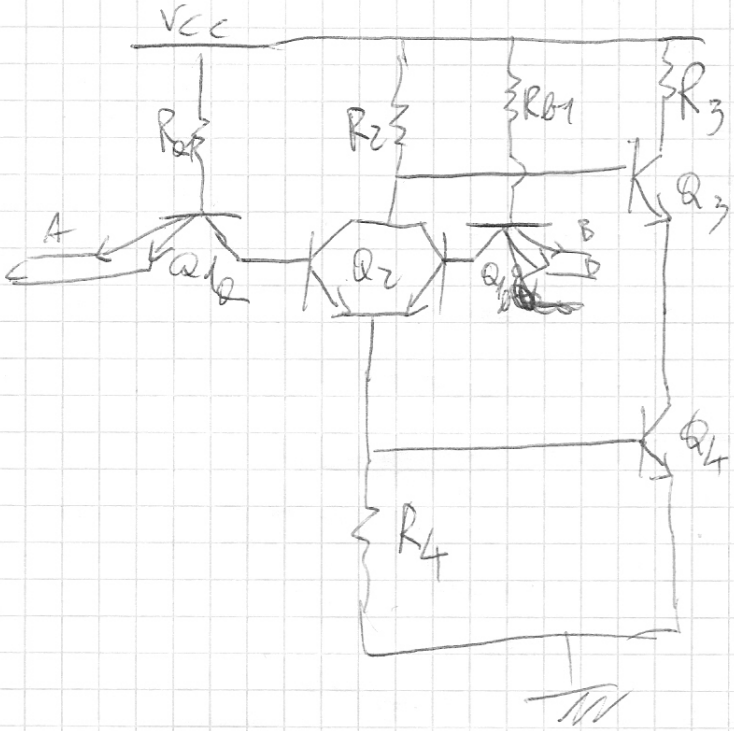
← CMOS

PSEUDO - NMOS



TTL

$Y = \overline{AC + BD}$



$V_{OL\,TYP}$ è la tensione tipica di output riconosciuta come livello basso

CMOS ed NMOS:

$V_{OL\,TYP} = 0\,V$

TTL

$V_{OL\,TYP} = 0{,}2\,V$

$V_{OL\,MAX}$ = massimo valore di tensione tale per cui l'uscita viene riconosciuta come livello basso

CMOS e NMOS:

$V_{OL\,MAX} = \frac{V_{DD}}{2}$

TTL

V_{OH} —— V_{IH} —— V_{IL} —— V_{OL} ——

~~$V_{OL\,max} = 0{,}8\,V$~~

$V_{OL\,max} = 0{,}4\,V$

$I_{OL\,max}$ corrente massima V_{in} uscita corrispondente a livello basso

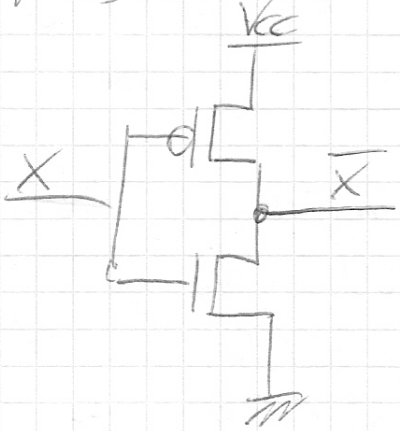
CMOS e NMOS

$I_{OL\,max}$ è dell'ordine dei pF ⇒ NM$_L$ è molto grande e viene limitato a 0

TTL

$I_{OL\,max} = 16\,mA$

NOT CMOS:



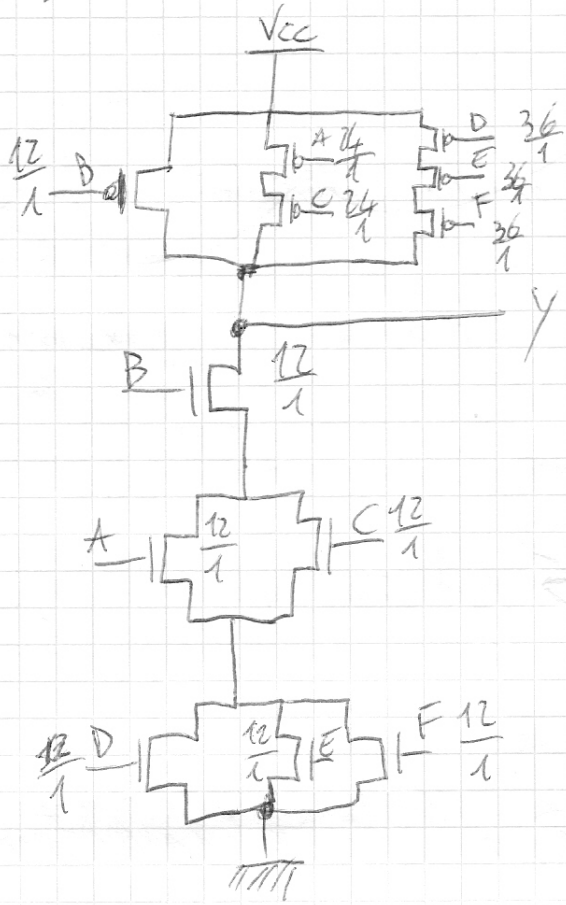
Per avere inverter più veloce ⇒ ho pezzo più grande

21/07/2008

③ $Y = \overline{B} + \overline{A}\overline{C} + \overline{D}\overline{E}\overline{F} = \overline{\overline{B} + \overline{A}\overline{C} + \overline{D}\overline{E}\overline{F}} =$

$= \overline{\overline{B} \cdot \overline{\overline{A}\overline{C}} \cdot \overline{\overline{D}\overline{E}\overline{F}}} = \overline{B \cdot (A+C) \cdot (D+E+F)}$

CMOS:



Il caso peggiore per i transistor ~~de~~ per i rami in parallelo è quello che contiene più transistor, mentre per i rami in serie ~~sono~~ ~~il ramo~~ dobbiamo considerare ~~uno dei casi~~ ~~casi~~ peggiori

Da H a L: $B=1, C=1, F=1, A=D=E=0$

Da L a H: $D=E=F=0, A=B=C=1$

⇒ Percorsi di caso peggiore sono:

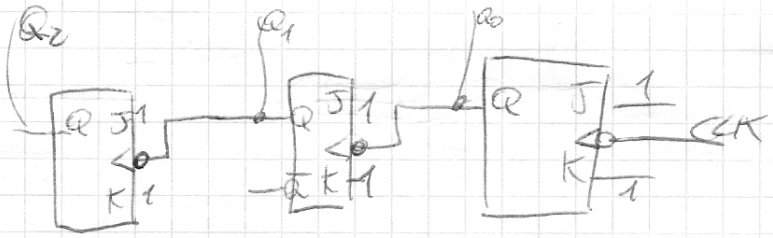
Da H a L: quelli che hanno
- uno tra A e C a 1
- uno tra D, E ed F a 1
- B = 1

Da L a H: quello che ha
D, E e F a 0

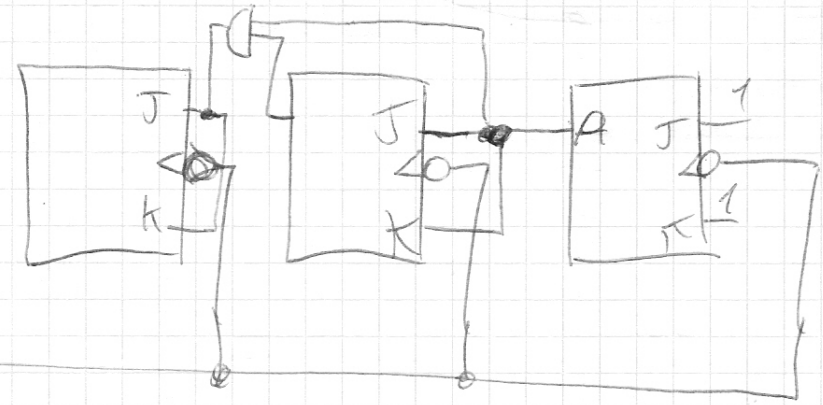
Il motivo è che ~~ogni transistor~~ abbiamo bisogno di considerare il percorso più lungo da percorrere per la carica/scarica. Ogni transistor è un carico resistivo

---

CONTATORE ASINCRONO:
MOD 8

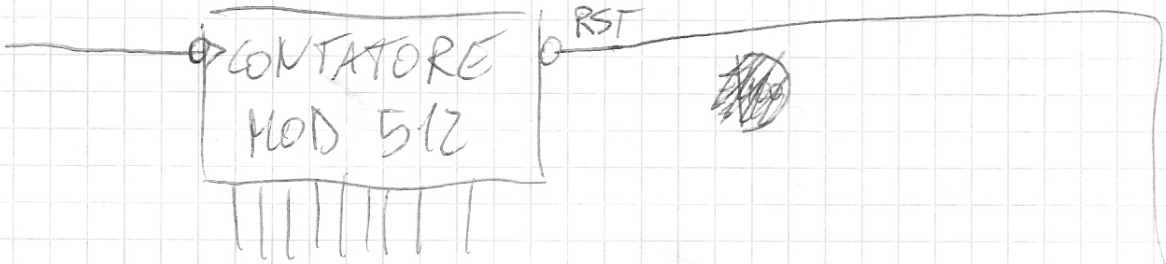


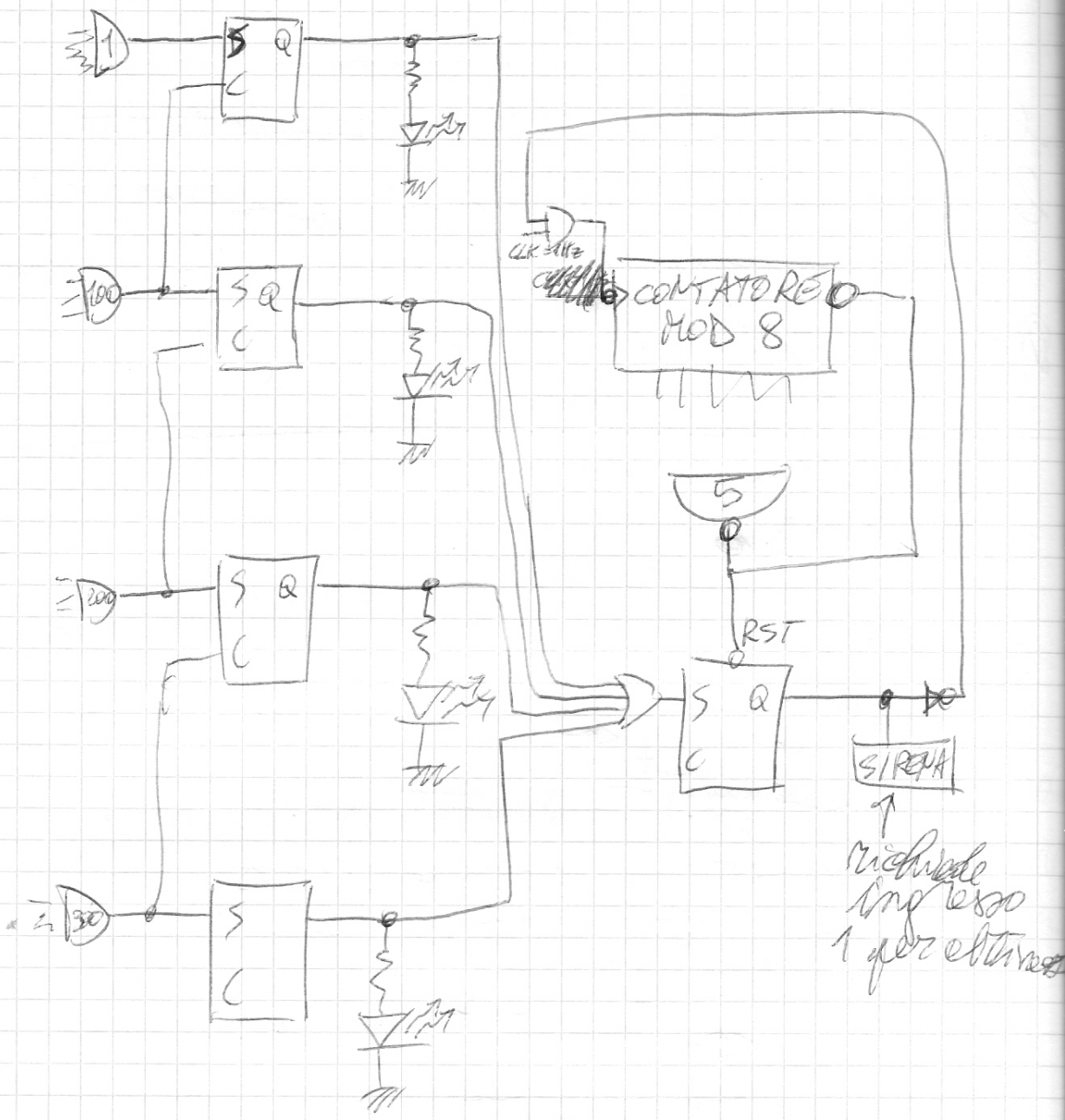
CONTATORE SINCRONO MOD 8

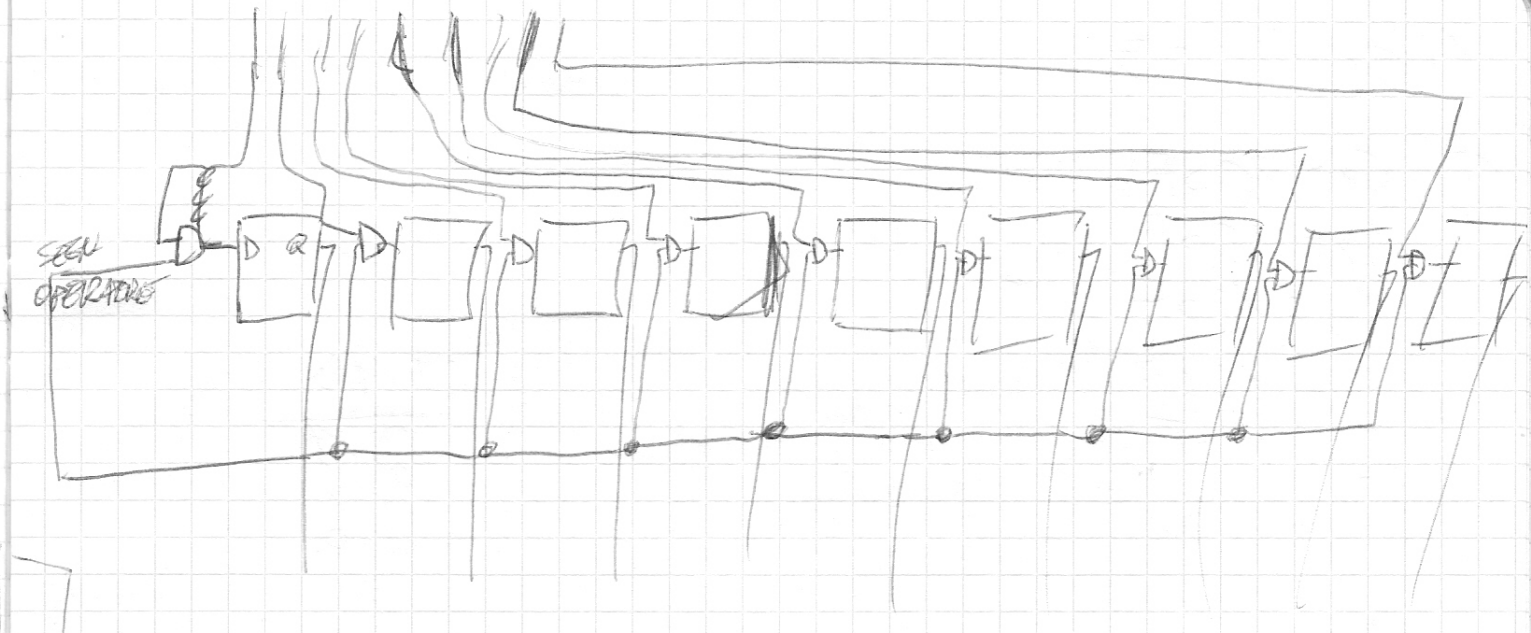


11/02/'08

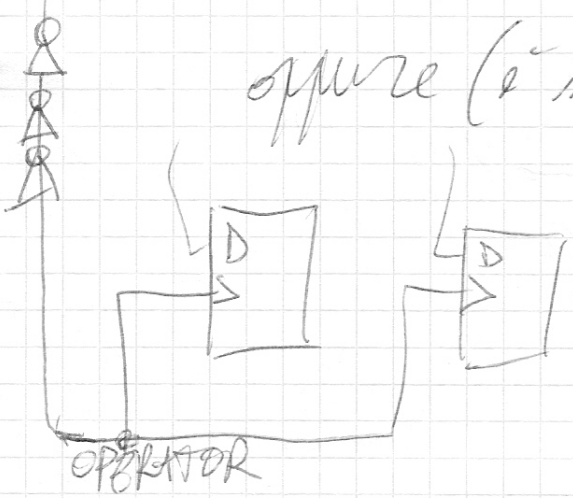
1


CONTATORE
MOD 512
RST

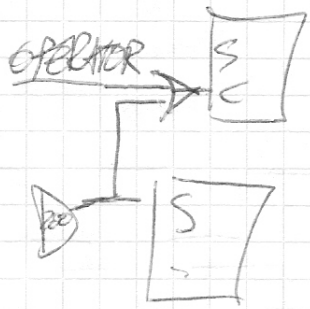

1
100
200
300
S
Q
C
CONTATORE
MOD 8
5
RST
SIRENA
richiede
tmp lesso
1 per attivare



oppure (è meglio)



e poi per esserne sicuri



512 256 128 64 32 16 8 4 2 1
2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

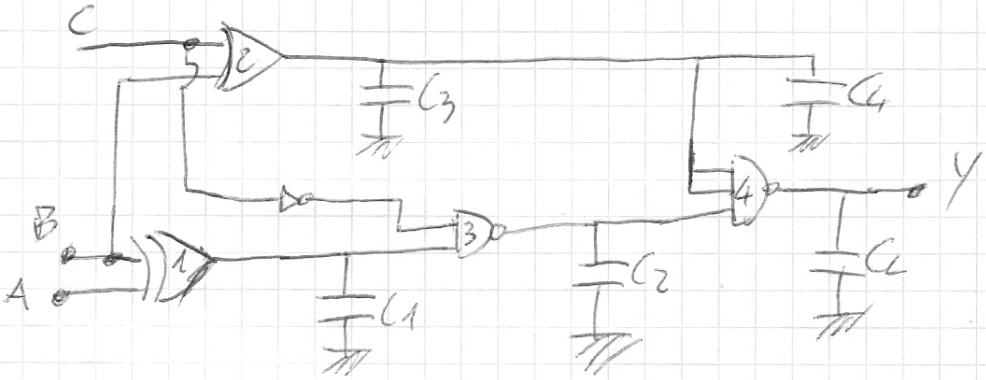
I H G F E D C B A
0 0 1 1 0 0 1 0 0

⇒ A
B
C
D
E
F
G
H
I

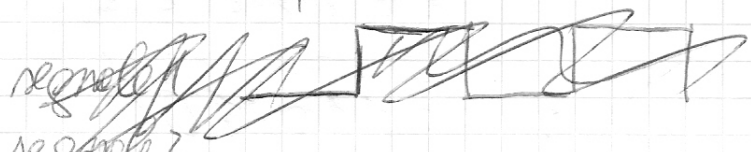
11/04/2003

③ $C_1 = 20pF$
$C_2 = 20pF$
$C_3 = 10pF$
$C_4 = 30pF$
$C_2 = 50pF$
$C_{inq2} = 5pF$

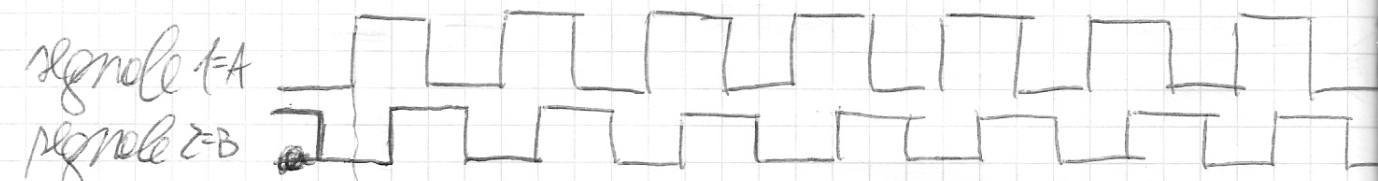
NAND	
00	1
01	1
10	1
11	0



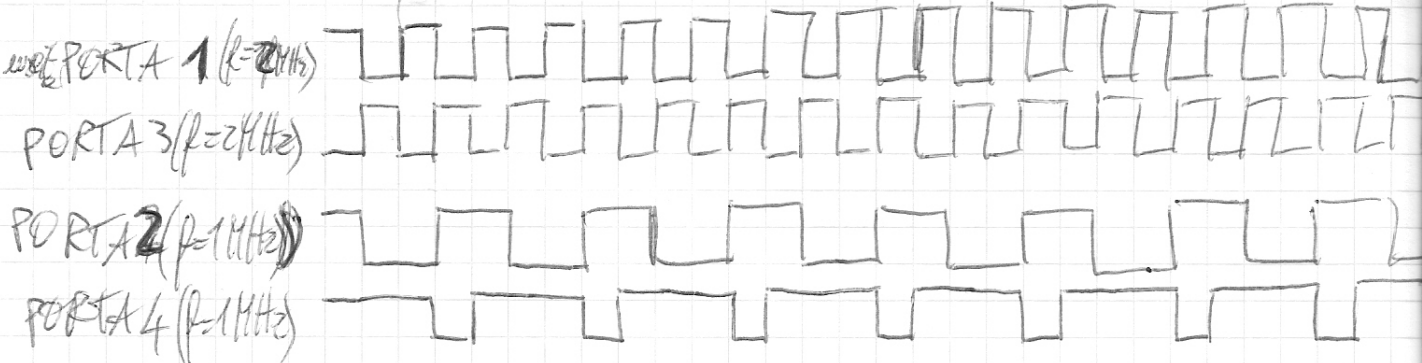
$f = 1MHz$
$T = 1\mu sec$
sfasato di $\frac{T}{4}$



segnale 2



segnale 1=A
segnale 2=B



uscita PORTA 1 (f=2MHz)
PORTA 3 (f=2MHz)
PORTA 2 (f=1MHz)
PORTA 4 (f=1MHz)

$$P_{DD_2} = V_{CC}^2 \cdot f_{OUT} \cdot (C_3 + C_{inq}) = 25 \cdot 1 \cdot 10^6 \cdot (10 \cdot 10^{-12} + C_{inq}) =$$
$$= 25 \cdot 10^6 \cdot (15 \cdot 10^{-12}) =$$
$$= 25 \cdot 15 \cdot 10^{-6}$$

$$P_{DD_1} = V_{CC}^2 \cdot f_{OUT} \cdot (C_1 + C_{inq}) = 25 \cdot 2 \cdot 10^6 \cdot (20+5) \cdot 10^{-12} =$$
$$= 625 \cdot 2 \cdot 10^{-6}$$

25·
25=

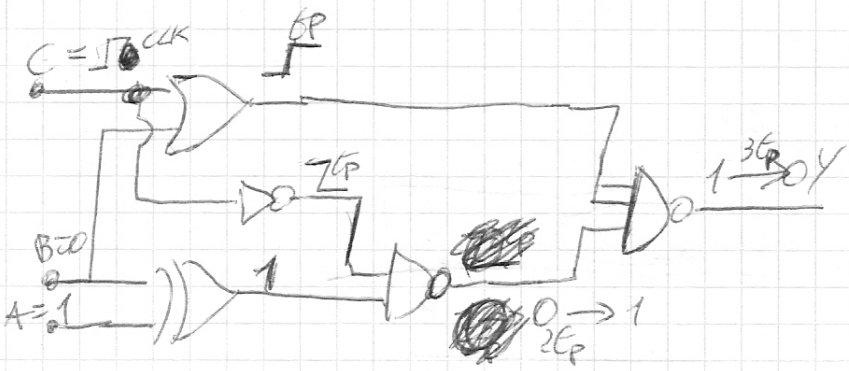
125
500
625/25
125/25

$$P_{DD_{NOT}} = 0$$

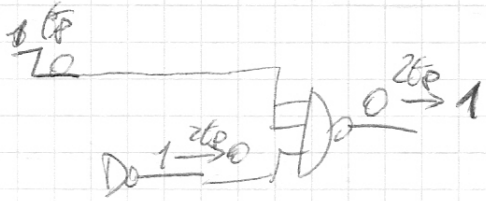
$$P_{DD_3} = V_{CC}^2 \cdot f_{OUT_3} \cdot (C_2 + C_{inq}) = 25 \cdot 2 \cdot 10^6 \cdot (20+5) \cdot 10^{-12}$$

$$P_{DD_4} = V_{CC}^2 \cdot f_{OUT_4} \cdot (C_L) = 25 \cdot 1 \cdot 10^6 \cdot 50 \cdot 10^{-12}$$

LH

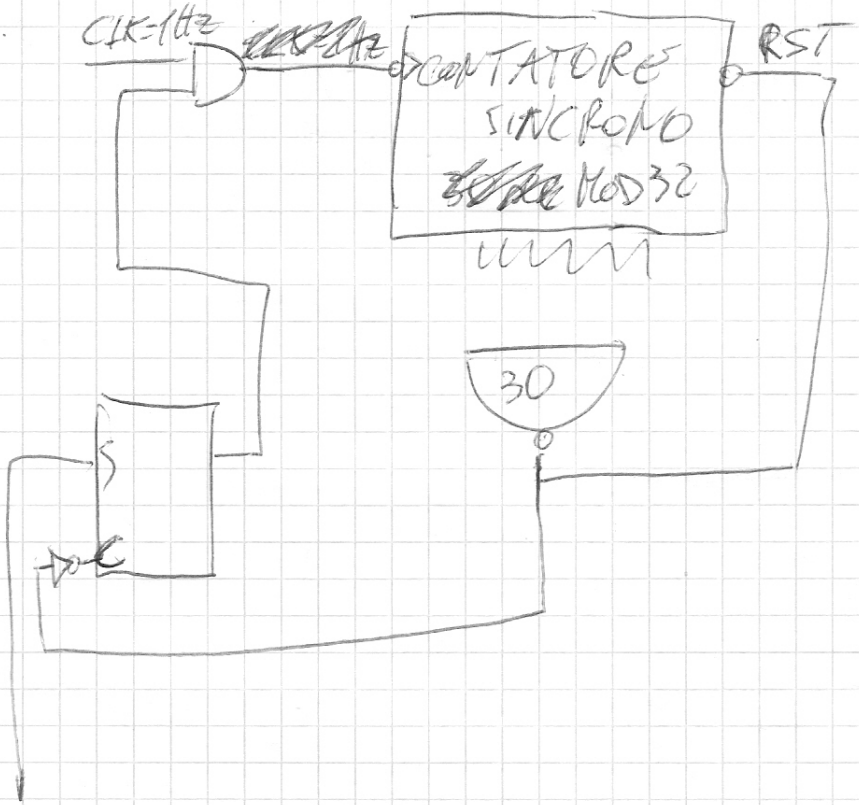


H-L

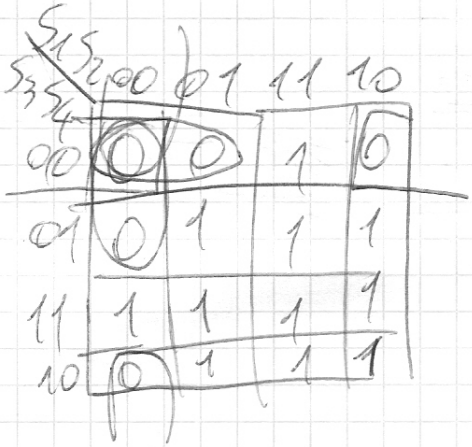


8/01/2008

③ ingressi $S_1 S_2 S_3 S_4$ uscita Y (attiva alta)



S_1	S_2	S_3	S_4	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



$$Y = (S_1 + S_3 + S_4) \cdot (S_1 + S_2 + S_3)(S_2 + S_3 + \cdot (S_1 + S_2 + S_4)$$